REMARKS

Claims 1-21 are currently active.

Antecedent support for the limitation of "packets of different lengths" is found on page 1, lines 9-13, and the amendment to Claims 1 and 7 is found in Claim 4.

The Examiner has rejected Claims 1-3 as being unpatentable over Cisneros in view of Gaddis and Koehler. In view of the amendments to the claims, applicants respectfully traverse this rejection.

Referring to Cisneros, there is disclosed a packet address look-ahead technique for use in implementing a high-speed packet switch. Cisneros teaches the switch is formed of interface modules 210, control and service modules 295, cross-connect 220, demultiplexers 230, multiplexers 280, switch fabric 250 and switch control module 290. See column 13, lines 30-38. As is clearly evident from figure 2 and from the teachings of Cisneros, there is only one single switch fabric 250.

The switch fabric 250 contains output modules 270, contention resolution unit 510 and self-routing cross-point planes 550. The input modules provide groups of

simultaneous incoming cells to self-routing cross-point plane 550 for simultaneous routing therethrough. Switching planes 550 are formed of multiple planes of self-routing cross-point circuits. See column 15, lines 4-15.

The switching planes 550 are not fabrics, as the examiner submits on page 7, paragraph 4 of section 4 of the Office Action, where the Examiner states "note that self-routing cross-point planes 550 are 'fabrics'". It is respectfully submitted it is improper for the Examiner to make this statement, and it is incorrect. The very teachings of Cisneros state that there is only one fabric 250. The fabric is comprised of cross-point planes 550 which are only one component of the fabric. The cross-point planes are not fabrics and to call them fabrics is completely contrary to the very teachings of Cisneros itself which clearly states the planes 550 are a part of the fabric 250. Furthermore, the cross-point plane is inherently not a plurality of fabrics, but a single element that is well known in the art to be non-blocking, as Cisneros teaches on column 15, line 16 and is one single complete circuit. Accordingly, Cisneros only teaches an architecture of the switch that uses one single fabric.

Referring to Gaddis, there is disclosed and ATM-Ethernet portal/concentrator. Gaddis teaches an ATM-Ethernet portal which conveniently connects disjoint Ethernet segments over an ATM/BISDN network creating one large logical Ethernet segment. See column 1, lines 33-37. Gaddis teaches the main components of the portal are a control

microprocessor 20, an Ethernet controller 22, an ATM cell processor, a dual-ported shared memory 24, and a DMA controller 26. See column 4, line 66-column 5, line 1. The Examiner states that Gaddis teaches a fabric in figure 3, on page 7, last paragraph of the Office Action. A review of figure 3 does not show anywhere a fabric, nor can applicants find where Gaddis specifically even mentions a fabric throughout the reference. Thus, neither Cisneros nor Gaddis teach or suggest anything regarding a plurality of "fabrics", as found in Claim 1 of applicants.

Furthermore, the Examiner suggests that the shared memory must have the functionality to locate/identify each frame by its size and refers to column 6, lines 61-64, as stated on page 8, first paragraph of the Office Action. A review of column 6, lines 61-64 simply states that the Ethernet controller can write incoming frames or read an outgoing frames, or the microprocessor can access data, concurrent with DMA transfers to and from the ATM cell processor. It is respectfully submitted this has nothing at all to do with the limitation of placing a linked indicator with a packet so when the packet is stored in the memory of the memory mechanism, the determining mechanism can identify from the length indicator how long the packet is and where the packet ends in the memory of the memory mechanism. The examiner is reading the limitation into the teachings of Gaddis because there may be many other ways that the Ethernet controller can read or write a frame, such as by the

fact that the frame is a fixed size and it just reads or writes the fixed length which is different from the aforementioned limitations in Claim 1.

Moreover, Claim 1 has the limitation that the packets are of different lengths, which Gaddis does not recognize whatsoever; and furthermore, the memory has a wide cache buffer structure in which the multiple packets are put into one word, which is nowhere taught or suggested in Gaddis.

Referring to Koehler, there is disclosed an apparatus and method for synchronization of multiple data paths and recovery from lost synchronization. Koehler teaches that 32-bit data packets are transferred to splitting circuitry 16 which splits each of the data packets into two 16-bit portions which are transferred along to respective parallel paths or pipes on 16-bit buses 18 and 20 for further processing. The splitting circuitry 16 also generates for each 16-bit portion of the data packet a synchronization code, also referred to as a sync code. As the splitting circuitry splits each data packet into two portions, which are referred to as a high portion and a low portion, it assigns to and couples with each portion a two-bit synchronous code. See column 5, lines 9-26.

Koehler teaches that after the data packets are split by the splitting circuitry, they can be processed by the circuitry that required the packet to be split. Such a circuitry is

identified generically in figure 1 as reference numeral 26 and 28. The circuitry 26, 28 can be packet switching circuits that cannot be implemented in 32-bit configurations because of pin count limitations. Thus, Koehler teaches that splitting in regard to the system taught by Koehler, means shortening the size of a the data being sent. See column 5, lines 28-34. This is not striping at all. Furthermore, Koehler fails to teach or suggest the use of fabrics of a switch. The circuitry 26, 28 are switches, not fabrics of switches.

After processing by the circuits 26 and 28, the packet portions are transferred along individual paths to the grouping circuitry 38. The grouping circuitry groups the incoming smaller packet portions back into the originally sized 32-bit packets. See column 5, lines 44-50. Koehler teaches that figure 2 shows the splitting circuitry 16. The 32-bit data packets are received and split into 2 16-bit data streams 42, 44 by a data splitter 46. The 16-bit data packet portions are afforded along the data streams 42, 44 to a high side data reformatter 52 and a low side data reformatter 54, respectively. The 18-bit data packages, which include the two-bit pcode bits are forwarded out of the splitting circuitry 16 toward the functional circuits 26 and 28. See column 5, line 53-column 6, line 2.

As is evident from the teachings of Koehler and the figures of Koehler, the functional circuits 26, 28 only receive full data from one splitting circuitry 16. There is no teaching or suggestion of each fabric receiving stripes of fragments of packets from each port

card as is found in applicants' invention of Claim 1. Accordingly, Koehler does not add anything to Cisneros or Gaddis in relevant part to applicants' invention of Claim 1.

Claim 1 now has the limitation that "the port cards sending stripes of corresponding fragments of each packet to the fabrics". The applied art of record does not teach or suggest anything in regard to striping, or striping of corresponding fragments, let alone sending stripes of corresponding fragments of each packet from each of the port cards to each of the fabrics, as found in Claim 1. At best, the applied art of record shows sending a smaller portion of a packet from a single port card to a single fabric, but nothing at all about stripes of corresponding fragments from more than to more than one fabric.

In regard to Koehler, the Examiner also submits that splitting or striping are one in the same. Respectfully applicants take strong difference to the statement. To one skilled in the art, striping is a very different and a very definite operation as compared to splitting. The functionality is not the same and the Examiner cannot equate striping and splitting as equivalent when one skilled in the art would not recognize them as the same. Applicants chose the term striping because that is the specific operation that they use to describe the operation of the claimed invention. Applicants are entitled to the common definition of the term striping, as understood by one skilled in the art, and for it to be given

deference. Accordingly, for this reason alone that Koehler teaches splitting and not striping, Koehler is not applicable to applicants' claimed invention.

In addition, it is well recognized patent law that there must be teachings in the applied art of record themselves to combine the specific teachings the examiner relies upon to arrive at applicants' claimed invention. Here, there is no teaching or suggestion in the applied art of record to combine Cisneros, Gaddis or Koehler. It is only with hindsight of applicants' claims themselves is there any basis for combining these references. However, hindsight is contrary to the law. It is submitted the Examiner is using applicants' claims as a road map to find all different elements and limitations in different references of the applied art, and having found each of the different elements or limitations in the different references, conclude that applicants' claimed invention is arrived at. Again, this is contrary to black letter patent law.

Furthermore, it is also black letter patent law that references cannot be taken out the context in which they are found. In regard Cisneros, there is taught a high-speed packet switch. In regard to Gaddis there is taught an ATM-Ethernet portal which connects disjoint Ethernet segments. The architectures described above for both of these references are completely different, and the purpose of these references are completely different. Similarly, in regard to Koehler there is taught a system and method for synchronizing transmission of data over multiple data paths. This again is completely different from the purposes and

architectures taught by Cisneros and Gaddis. There is no reason why one skilled and the art would look to Cisneros or Gaddis or Koehler to combine any of the teachings of one into the other. Very are completely distinct and essentially have nothing to do with each other. Moreover, if one skilled in the art, were even to try to combine any of these references would have to redesign and put significant amount of research and development time into somehow or other making the systems or architectures taught by each of the references to be somehow compatible with the teachings of the other references to somehow make use of the different elements and limitations the Examiner suggests arrive at applicants' claimed invention. In fact, applicants respectfully submit there is no reason why one skilled in the art would take the reference of Cisneros and its teachings and look to some type of a ATM/Ethernet portal to modify the teachings of Cisneros, or to look to the teachings of Koehler in regard to an overall system to modify both Gaddis and Cisneros to be able to use the specific teachings the Examiner relies upon to arrive at applicants' claimed invention. It is respectfully submitted no one skilled in the art would do this. Accordingly, Claims 1-3 are patentable over Cisneros in view of Gaddis and Koehler.

The Examiner has rejected Claims 4-6 as being unpatentable over Cisneros and Gaddis, Koehler and Joffe. Applicants respectfully traverse this rejection.

Referring to Joffe, there is disclosed a memory interface unit, shared memory switch system and associated method. Joffe teaches first multi-port shared memory system 18. The system 18 includes a set of K ports 20 each inputing/outputing m-bit data words and n-word bursts, an interconnection matrix circuit 22, a set of m memory access buffers 24 in a shared memory 26. See column 5, lines 12-15. Joffe teaches each memory access buffer 24 is dedicated to storing a specific position for every data word transferred through any of the ports. See column 5, lines 48-54. The Examiner submits on page 11, paragraph 3 of section 5 that Joffe teaches the limitation of a memory which has a wide-cache buffer structure in which multiple packets are put into one word and refers to column 5, lines 46-67 of Joffe to support this contention. A review of column 6, lines 46-67 was referred to in the previous sentence and simply refers to the fact that each buffer is responsible for a single bit position in every word, See column 5, line 55. It is respectfully submitted that nowhere does column 6, lines 46 to 67 teach or suggest the limitation of a wide cache buffer structure in which multiple packets are put into one word.

Furthermore, as explained above, the architecture taught by Joffe has nothing at all to do with the architectures taught in Cisneros Gaddis or Koehler. They are not compatible, or if it was even attempted to make them compatible, would require significant research and development by one skilled and the art to make them compatible. In other words, there is no enablement in regard to how to take the different contexts of all these

different references and somehow or other combine them to make them work. There is no reason to combine these references, except from the hindsight of applicants' claims. The applied art of record does not teach or suggest the limitations of Claim 1. Claims 4-6 are dependent to parent Claim 1 and are patentable for the reasons Claim 1 is patentable.

The Examiner has rejected Claims 7-15 as being unpatentable over Cisneros in view Gaddis in view of Koehler. As explained above in regard to Claim 1, Cisneros in view of Gaddis does not teach or suggest Claim 1, as amended. Claim 7 is patentable for the reasons Claim 1 is patentable over the applied art of record. Claims 8-15 are patentable for the reasons Claim 7 is patentable.

The Examiner has rejected Claim 16 as being unpatentable over Cisneros and Gaddis, Koehler and Jones. Applicants respectfully traverse this rejection. Cisneros and Gaddis and Jones do not teach or suggest the limitations of Claim 1 or Claim 7. Claim 16 is dependent to parent Claim 7 and is patentable for the reasons Claim 7 is patentable.

The Examiner has rejected Claims 17-21 as being unpatentable over Cisneros, Gaddis, Koehler, Jones and Joffe. Applicants respectfully traverse this rejection. Claims 17-21 are dependent to parent Claim 7 and are patentable for the reasons Claim 7 is patentable over the applied art of record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-21, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on 12/8/04

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